Sub-Thermal Subthreshold Characteristics in Top–Down InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs

Xin Zhao, *Student Member, IEEE*, Alon Vardi, *Member, IEEE*, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— This letter demonstrates top-down InGaAs/InAs heterojunction vertical nanowire tunnel FETs with sub-thermal subthreshold characteristics over two orders of magnitude of current. A minimal subthreshold swing of 53 mV/decade at $V_{ds} = 0.3$ V has been obtained at room temperature. An I_{60} (defined as the highest current level where the subthreshold characteristics exhibit a transition from sub- to super-60 mV/decade behavior) of 4.3 nA/μm has been achieved at $V_{ds} = 0.3$ V. Compared with an earlier device generation, much reduced temperature dependence of the subthreshold characteristics is observed in this letter. The major difference between the two device generations is the drastically reduced interface trap density, evidenced by the improvement in the subthreshold swing of InGaAs vertical nanowire MOSFETs fabricated at the same time. This result suggests oxide–semiconductor interface trap-assisted tunnelling the main leakage mechanism in III-V TFETs fabricated by our process. The improvement in the interface quality has been enabled by improved gate oxide deposition and post-deposition treatment.**

***Index Terms*— TFETs, III-Vs, nanowire, InGaAs, InAs, heterojunction, top-down, vertical channel.**

I. Introduction

THE tunnel FET (TFET) has emerged as a promising technology for ultra-low power logic due to its ability to achieve a subthreshold swing (S) below 60 mV/dec at room temperature (RT), a physical limit to MOSFETs [1]. A lower subthreshold swing enables a reduction in supply voltage and lower system power consumption, crucial to a power-constrained environment for mobile, medical and internet of things applications. III-V semiconductors, including InGaAs, InAs and GaSb, are attractive materials to implement TFETs because of the flexible bandgap engineering that is possible and the potential to deliver high performance as a result of their direct bandgap and small effective mass [2].

To enable continuous scaling in the nanometer regime, a nanowire (NW) transistor geometry with wrapped-around gate is highly favorable due to its strong charge control and robustness to short-channel effects [3]. Compared to conventional horizontal devices, a vertical channel is a natural choice for III-V TFETs to fully leverage the bandgap engineering capabilities of III-V heterostructures. Furthermore, a vertical geometry can occupy smaller area from a circuit-level perspective [4]. Therefore, III-V vertical nanowire (VNW) TFETs are widely regarded as strong competitors to Si MOSFETs at low supply voltages [5]–[7].

Experimental TFET demonstrations to date, including III-V VNW architectures, have fallen short of theoretical predictions and failed to deliver sub-thermal switching at current levels high enough to be competitive with Si MOSFETs [2]. A particular manifestation of non-ideal behavior of TFETs is the significant temperature dependence of their subthreshold characteristics [8], [9]. This shoulds not be the case if band-to-band tunneling is the dominant current transport mechanism. This strong T dependence has been attributed to a tunnel-enabled carrier generation process through oxide/semiconductor interface trap states involving phonons [10], [11]. It is therefore of paramount importance to demonstrate III-V nanowire TFETs with minimal T dependence, steep subthreshold and high I_{60} (the highest current level where the subthreshold characteristics exhibit a transition from sub- to super-60 mV/dec behavior) [12], [13].

In this work, we present improved InGaAs/InAs heterojunction vertical nanowire (VNW) TFETs with sub-thermal subthreshold behavior and drastically reduced temperature dependence in the subthreshold regime, compared to an earlier device generation [9]. This weak temperature dependence mainly stems from a better oxide/semiconductor interface with much reduced interface trap density (D_{it}), as confirmed by the near-ideal linear S of InGaAs VNW MOSFETs fabricated at the same time. In combination with a drain underlap, we are able to achieve sub-thermal S over two orders of magnitude of current and a minimal S of 53 mV/dec at $V_{ds} = 0.3$ V and room T. Owning to the reduced tunnel barrier of the InGaAs/InAs heterojunction, an I_{60} of 4.3 nA/μm at $V_{ds} = 0.3$ V is obtained, which is one of the highest values demonstrated in experimental TFETs.

II. Experiment

Fig. 1 shows the schematic cross-section of our latest generation of VNW TFETs. The starting heterostructure was identical to that used in our previous work [9]. The tunnel

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The authors are with the Massachusetts Institute of Technology, Cambridge, MA 02142 USA (e-mail: xinzhao@mit.edu).

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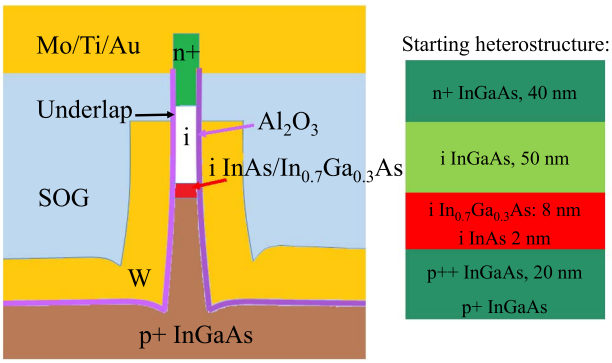

Fig. 1. Schematic of device structure and starting heterostructure.

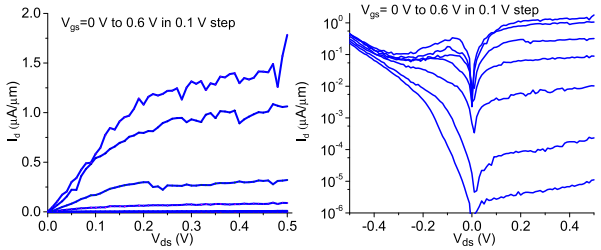

Fig. 2. Room temperature output characteristics of an exemplary VNW TFET in linear scale (left) and in semilog scale (right).

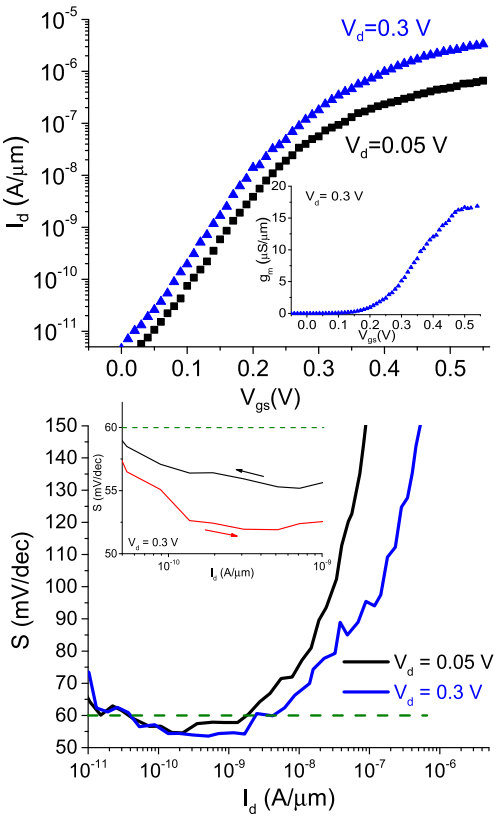

Fig. 3. Subthreshold and g_m characteristics (top) and subthreshold swing vs. I_d characteristics (bottom) of InGaAs VNW TFET, inset shows hysteresis behavior at $V_{ds} = 0.3$ V.

junction is located between the p^{+-} and i-$In_{0.53}Ga_{0.47}As$ layers where a 2 nm i-InAs/8 nm i-$In_{0.7}Ga_{0.3}As$ 'notch' has been inserted to boost the ON current [14].

Device fabrication followed our previous work [9] but with greater attention to ALD conditioning to improve the quality of the oxide/semiconductor interface. After RIE etching [15], 5 cycles of digital etch [16] were performed in order to trim the nanowire diameter (D) by 20 nm and improve the quality of the interface [15], [16]. A 15 nm drain underlap at the top of the nanowire was introduced to improve the subthreshold characteristics. A drain underlap reduces the electric field at the drain-gate junction that promotes ambipolar tunnel leakage, leading to sharper subthreshold characteristics [3]. A rapid thermal annealing (RTA) step at 350 °C for 3 min in N_2 environment was performed at the very end of the process to further improve the oxide/semiconductor interface quality. The final device features a single nanowire with channel length of 60 nm, D = 40 nm and 3 nm Al_2O_3 (EOT ~ 1.5 nm).

III. Results and Discussion

Fig. 2 shows the output characteristics of a representative device in linear scale on the left and in semilog scale including the negative V_{ds} regime on the right. The linear output characteristics exhibit good saturation. Clear negative differential resistance was observed for $V_{ds} < 0$ and high V_{gs}, confirming the tunneling nature of device operation in the ON regime. At $V_{gs} = 0.6$ V, we obtain a peak-to-valley ratio of 3.4. The drain current fluctuations in Fig. 2 are attributed to discrete charge trapping events via the very few oxide and interface defects that are present in a single NW device due to its extremely small channel dimension [17].

The subthreshold and g_m characteristics of the device in Fig. 2 are shown in Fig. 3 (top). A peak g_m ($g_{m,pk}$) of 17 μS/μm was obtained at $V_{ds} = 0.3$ V and DIBL is 102 mV/V. This is to be compared with $g_{m,pk} = 8$ μS/μm and DIBL = 320 mV/V in our previous work [9], despite a thicker oxide thickness here.

To take a closer look at the subthreshold characteristics, the subthreshold swing vs. drain current is plotted in Fig. 3 (bottom). A minimum S of 55 mV/dec was observed at $V_{ds} = 0.05$ V and was further reduced to 53 mV/dec at $V_{ds} = 0.3$ V. The slight improvement of S with drain bias might be due to an increase in gate efficiency as a result of the enhanced depletion of channel charge by the higher drain bias. Inset of Fig. 3 (bottom) shows small hysteretic behavior at $V_{ds} = 0.3$ V. Sub-thermal characteristics are observed in both sweeping directions. All these observations were made on multiple devices. At $V_{ds} = 0.3$ V, the subthreshold swing remains sub-thermal for over two orders of magnitude of current, delivering an I_{60} as high as 4.3 nA/μm.

In Fig. 4 (top), the subthreshold characteristics at $V_{ds} = 0.05$ V are shown at different T from liquid nitrogen to RT. Apart from a positive threshold voltage shift with decreasing temperature, the subthreshold swing shows minimal change as a function of temperature. This is evidenced in Fig. 4 (bottom) (the green stars) where S at $V_{ds} = 0.05$ V is plotted against T at constant current, 10^{-10} A/μm. The minimum subthreshold swing behaves in the same way with temperature.

In Fig. 4 (bottom), we also include data for a previous TFET generation [9] (S extracted at I_d of 10^{-10} A/μm) as well as an

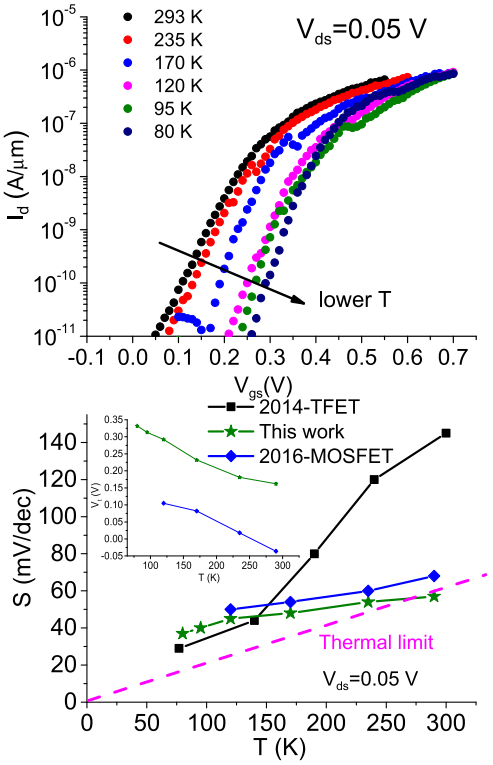

Fig. 4. Temperature dependence of subthreshold characteristics at $V_{ds} = 0.05$ V (top) and S at $V_{ds} = 0.05$ V at constant current level as a function of temperature (bottom) for TFET in this work, an InGaAs VNW MOSFET fabricated at the same time and a TFET from an earlier generation [9]. S extracted at I_d of 10^{-10} A/μm for TFETs and 10^{-9} A/μm for MOSFETs. Inset in the bottom figure graphs V_t vs. T in MOSFET and TFETs.

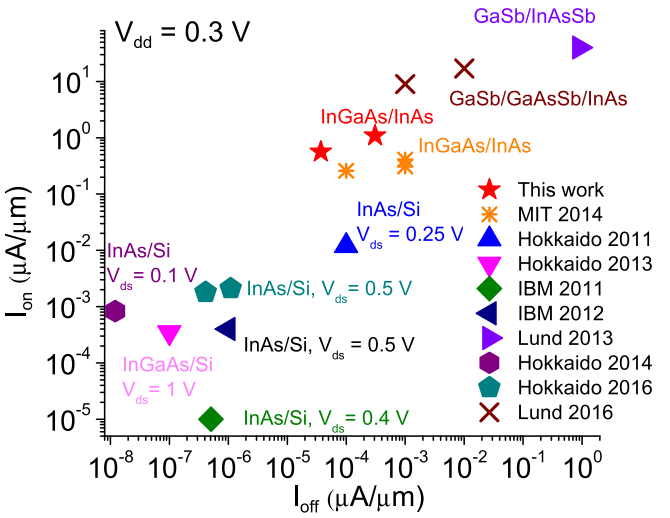

Fig. 5. I_{on} vs. I_{off} at $V_{dd} = 0.3$ V ($V_{ds} = 0.3$ V, $\Delta V_{gs} = 0.3$ V with exceptions marked next to data points) for recently published vertical III-V NW TFETs. All devices but the present ones are fabricated through bottom-up techniques.

InGaAs VNW MOSFET (S extracted at I_d of 10^{-9} A/μm) that was fabricated side-by-side with the current TFETs (dry etch, digital etch and ALD processes were performed in the same tools at the same time) and that has an identical D. While S in our previous TFET generation had a significant T dependence, changing from 145 to 30 mV/dec (RT to 77K), it only varies from 55 to 37 mV/dec over the same T range in this work.

The major difference between the two device generations is a significant decrease in the interface trap density (D_{it}). This is confirmed by the reduction in the subthreshold swing of the VNW MOSFETs that were fabricated with the TFETs, from 145 [15] to 65 mV/dec, as shown in Fig. 4 (bottom). This decrease in S can be translated into a reduction in D_{it} level according to $S = 60 \times (1 + q \times D_{it} \times t_{ox}/\varepsilon_{ox})$, where q is elemental charge, t_{ox} and ε_{ox} are the gate oxide thickness and dielectric constant, respectively. A tenfold decrease in D_{it} ($\sim 10^{13}$ to $\sim 10^{12}$ $eV^{-1}cm^{-2}$) is obtained as a result of better ALD chamber conditioning and post-deposition RTA. This comparison confirms a connection between a significantly reduced D_{it} level and the suppression of the T dependence of S. This, in turn, supports the hypothesis that the thermal signature of the subthreshold characteristics in [9] can be attributed to oxide/semiconductor interface trap-assisted tunneling (TAT), the rate of which is directly proportional to D_{it} [10], [11].

Besides TAT, the residual weak T dependence of S that is observed here might also be due to the presence of band tails in the channel [10]. This would affect TFETs as well as MOSFETs in a similar way. It is worth noting that the minimal S in Fig. 4 (bottom) for both generations of TFETs keeps improving with decreasing T into the liquid-N_2 range, highlighting the potential of obtaining a true tunneling steepness sharper than 37 mV/dec. The positive shift in threshold voltage that is observeds for both TFETs and MOSFETs is also consistent with the role of band tails although it could also be affected by residual doping [10] or oxide traps. Detailed modeling studies are required to confirm the origin of V_t shift.

Fig. 5 benchmarks I_{on} vs. I_{off} among published vertical NW TFETs [6], [7], [9], [13], [18]–[21], based on III-V materials at $V_{dd} = 0.3$ V ($V_{ds} = 0.3$ V, $\Delta V_{gs} = 0.3$ V). Several points in this figure have other V_{ds} values as marked due to data availability. Fig. 5 is designed to capture the tradeoff between dynamic switching speed and standby power. Compared to other vertical III-V NW TFETs, the top-down approach demonstrated in this work yields an excellent combination of steep slope and ON performance, delivering high I_{on} at low I_{off}.

IV. Conclusions

We have demonstrated top-down InGaAs/InAs heterojunction VNW TFETs with sub-thermal subthreshold behavior over two orders of magnitude of current at RT. These characteristics stem from improved oxide/semiconductor interface. The reduction in the interface trap density has also led to the suppression of a significant temperature dependence in the subthreshold characteristics that was observed in a previous device generation. This suggests the importance of interface trap-assisted tunneling as a dominant leakage mechanism in our III-V TFETs and the possible role of band tails when TAT is suppressed.

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